CLAIMS:

1. A method comprising:

coupling a tester to a buffer chip that is located on a DIMM using a first set of pins on the buffer chip;

coupling a plurality of DRAM modules that are located on the DIMM to a second set of pins on the buffer chip; and

testing the plurality of DRAM modules.

2. The method of claim 1, wherein coupling the tester to the buffer chip that is located on the DIMM using the first set of pins comprises coupling the tester to a first set of pins that carries differential signals during a non-test operation mode of the buffer chip.

3. The method of claim 2, wherein testing the plurality of DRAM modules comprises:

bypassing the buffer chip.

4. The method of claim 3, wherein bypassing the buffer circuit comprises:

connecting each of the first set of pins directly to a corresponding one of the second set of pins with a switching circuit.

5. The method of claim 4, wherein the switching circuit comprises one selected from the group consisting of a passgate circuit and an inverter circuit.

6. The method of claim 5, wherein bypassing the buffer circuit further comprises:

disabling an internal clock signal generated by a phase-locked loop in the buffer chip.

7. The method of claim 2, wherein testing the plurality of DRAM modules comprises:

mapping the first set of pins to corresponding ones of the second set of pins using a circuit of the buffer chip that is used during the non-test operation mode.

8. The method of claim 7, wherein mapping the first set of pins to corresponding ones of the second set of pins comprises:

passing command, address, and data signals to the plurality of DRAM modules after introducing an internal delay in the buffer chip.

9. The method of claim 8, wherein introducing the internal delay in the buffer chip comprises introducing an internal delay of one DRAM clock cycle.

10. The method of claim 9, wherein introducing the internal delay of one DRAM clock cycle comprises:

clocking a first half of a data word from the tester to a DRAM module on a rising edge of a clock signal; and

clocking a second half of the data word to the DRAM module on a falling edge of the clock signal.

11. The method of claim 8, wherein introducing the internal delay in the buffer chip comprises introducing an internal delay of two DRAM clock cycles.

12. A memory device comprising:

a plurality of DRAM modules;

an edge connector, wherein the edge connector is configured to accommodate a DRAM tester; and

a buffer chip with a first set of pins coupled to the plurality of DRAM modules and a second set of pins that are coupled to the edge connector.

13. The device of claim 12, the buffer chip further comprising:

a switching circuit configured to couple one of the first set of pins directly to one of the second set of pins, thereby bypassing the other circuits in the buffer circuit.

14. The device of clam 13, the switching circuit chosen from the group consisting of a passgate circuit and an inverter circuit.

15. The device of claim 13, the buffer chip further comprising:

a phase-locked loop circuit; and

a multiplexer configured to select from among at least two clock signals, wherein a first one of the at least two clock signals is an output of the phase-locked loop circuit.

16. The device of claim 15, a second one of the at least two clock signals comprising an input of the phase-locked loop circuit.

17. The device of claim 15, the second one of the at least two clock signals comprising an output of a logic circuit, wherein inputs of the logic circuit comprise an input of the phase-locked loop circuit and at least one additional clock input from the DRAM tester.

18. The device of claim 17, the logic circuit comprising XOR logic gates.

19. A system comprising:

a host that includes a processor;

a memory bus; and

a plurality of memory devices, the host and the plurality of memory devices connected to the memory bus in a point-to-point manner, each memory device having a plurality of DRAM devices and a buffer chip with a first interface between the buffer chip and the memory bus and a second interface between the buffer chip and the plurality of DRAM devices, the buffer chip configured to connect a first interface pin to a second interface pin during a test mode of operation.

20. The system of claim 19, the buffer chip comprising:

a switching circuit configured to directly connect the first interface pin to the second interface pin.

21. The system of claim 20, the switching circuit comprising:

a switching circuit selected from the group consisting of a passgate circuit and an inverter circuit.

22. The system of claim 19, the buffer chip comprising:

a phase locked loop circuit; and

a switch circuit configured to select one from the group consisting of an external reference clock and an output of the phase locked loop circuit.

23. A machine-readable medium, that when read, causes a machine to perform processes comprising:

establishing a signal path between an edge connector of a DIMM and a DRAM module located on the DIMM, wherein the signal path lies through a buffer chip.

24. The machine-readable medium of claim 23, wherein establishing the signal path between the edge connector of the DIMM and the DRAM module comprises:

connecting a first pin on the buffer chip and a second pin on the buffer chip, wherein the first pin and the second pin are normally configured to transfer data at different speeds.

25. The machine-readable medium of claim 24, wherein connecting the first pin on the buffer chip and the second pin on the buffer chip comprises:

operating a switch circuit that directly connects the first pin to the second pin.

26. The machine-readable medium of claim 25, wherein the switch circuit is one chosen from the group consisting of a passgate circuit and an inverter circuit.

27. The machine-readable medium of claim 24, wherein connecting the first pin on the buffer chip and the second pin on the buffer chip comprises:

inserting a delay that is equal to at least one DRAM clock cycle between the first pin and the second pin using a circuit on the buffer chip.